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EXAMINER	
LIN, WEN TAI	

ART UNIT	PAPER NUMBER
2154	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTO-INBOX@AKACHANLAW.COM

Office Action Summary	Application No.	Applicant(s)	
	10/708,503	CHEN ET AL.	
	Examiner	Art Unit	
	Wen-Tai Lin	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 45-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 45-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 and 45-67 are presented for examination. Claims 45-67 are newly added.

2. It is noted that the statuses of claims 45-67, which are shown to be "Previously Presented", are incorrect. These claims are considered new as of 6/24/08 because the earlier submittal on 5/30/08 was not entered. However, Applicant does not need to do anything to correct the status because it will automatically advance to the "Previously Presented" state following this office action.

3. Claims 56-58 are objected to because the term "the network port" in these claims appears to lack antecedence basis.

4. The text of those sections of Title 35, USC code not included in this action can be found in the prior Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 45-47, 56-58 and 61-63 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Specifically, the following features included in 45-47, 56-58 and 61-63 are not found in the specification (including those incorporated by reference):

(i) "analog-to-digital converter", "analog input" and "digital-to-analog converter" in claims 45-47, respectively;

(ii) "providing a scale-down factor" for scaling down the first/second time stamps, etc. in claims 56-58; and

(iii) "phase-locked loop" in claims 61-63.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 50-55 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Specifically, these new claims added new subject matter, though could be found in the specification, in a way that they may or may not be relevant to their respective parent claims. For example, claim 50 may be related to claim 1 if the received first entry is part of the received

traffic from the network in claim 1. However, the received "first entry" could also be interpreted as any other information irrelevant to the traffic data included in claim 1. Applicant is reminded that adding subject matter outside the existing classified class/subclass may be further restricted and withdrawn by default. In the example of claim 50, it could have been classified in various classes such as 704 (signal processing), 711 (memory structure) or 707 (data structure) if the added features are not closely related to the existing traffic management (already classified in 709/224).

The same aforementioned issue applies to dependent claims 51-52 versus their parent claims 8-9. Likewise, the similar issue applies to claim pairs (53, 1), (54, 8) and (55, 9).

In stead of imposing a restriction right now, Applicant is given a chance to further correlate the features of claims 51-55 to their respective parent claims so that they may not be broadly interpreted as unrelated subject matter, thereby avoiding a further restriction.

Claim Rejections - 35 USC § 103

8. Claims 1-6, 8-9, 48 and 59-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al.(hereafter "Lee") [U.S. PGPub 20030152084].

9. As to claims 1-2, Lee teaches the invention substantially as claimed including: a method of managing traffic over a network comprising:

receiving incoming traffic from the network in a digital signal processing integrated circuit having at least 128K bytes of on-chip memory [e.g., paragraphs 19 and 74-75; i.e., each MISD processor has 32 x 64K bytes of instruction memory and 64K registers];

performing a policing function on the incoming traffic to the digital signal processing integrated circuit in a first core of the digital signal processing integrated circuit [e.g., 220a, Fig. 4, paragraph; 76, wherein the first MISD processor (PCU) performs traffic policing];

performing a congestion control function in a second core of the digital signal processing integrated circuit, wherein the second core processes data generated by the first core [e.g., 220b, Fig.4 (i.e., TPU); paragraph 76; note that result of process 222a is fed to its following process 222b]; and

performing a shaping function in a fourth core of the digital signal processing integrated circuit, wherein the fourth core processes data generated by the third core [e.g., 220c (i.e., FPU), Fig.4; paragraph 76].

Lee teaches that the scheduling function in the second core of the digital signal processing integrated circuit together with the congestion control function [paragraph 76]. Lee does not suggest performing the scheduling function in a separate core (i.e., the third core of the digital signal processing integrated circuit).

However, based on Lee's modular MISD arrangement, it is obvious to one of ordinary skill that the system may be extended to more than the three-stage processors (as illustrated in Fig. 4). For example, when it is perceived that traffic scheduling takes up a big chunk of processing time the MISD a different MISD processor, an ordinary skilled artisan could have dedicated a third MISD in the pipe for the job because the approach is predictable and the

advantage of alleviating processing bottle-neck using additional MISD is obvious. See KSR, 127 S. Ct. at 1742, 82 USPQ2d at 1397.

Further, Lee does not specifically teach that the four-stage MISD processors are implemented in a digital signal processing integrated circuit.

However, it is well known, at the time the invention was made, that advanced IC fabrication technology could fit multi-million-transistors on a single chip. High density interconnection technology to integrate multiple processor dies onto a single integrated chip package is also available. It would have been obvious to one of ordinary skill in the art to have integrated Lee's four MISD processors into a single digital signal processing circuit because it reduces the overall physical size of the processors and parasitic capacity due to wirings (i.e., potentially makes the system running at a higher speed).

10. As to claim 3, Lee further teaches that a traffic management function comprises sorting the traffic by class of service, policing traffic to not exceed boundary of a bandwidth of the channel, and scheduling traffic [e.g., paragraphs 24-25 and 76; Fig. 38] .

11. As to claim 4, Lee further teaches that the scheduling traffic is based on priority queuing, first in first out queuing, class based queuing, round robin, waiting round robin, earlier deadline first, weighted fair queue, deficit round robin, or modified deficit round robin [e.g., paragraphs 261 & 344; note that inherently a queue is order as first-in-first-out].

12. As to claim 5, Lee further teaches that there is no direct communication path between the first core and the second core [e.g., paragraphs 83-84, i.e., the MISD processors are interconnected through buffers or external memory].

13. As to claims 6, 48 and 59-60, Lee further teaches that the data generated by the first core is passed to the second core using a mailbox [e.g., paragraph 84, i.e., "the DBU 292 stores the fixed size buffers into memory and other functional units (such as the FPU) have access to those buffers."].

14. As to claims 8-9, since the features of these claims can also be found in claims 2, they are rejected for the same reasons set forth in the rejection of claims 2 above.

15. Claims 7, 49 and 64-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al.(hereafter "Lee")[U.S. PGPub 20030152084], as applied to claims 1-6 and 8-9 above, further in view of Bass et al.(hereafter "Bass")[U.S. Pat. No. 6769033].

16. As to claims 7 and 49, Lee teaches that the MISD processor is a data flow machine that is triggered by the availability of data [e.g., paragraphs 73]. Thus, when a plurality of MISD processors are interconnected as shown in Fig. 4, processors (such as 220a – 220c) are synchronized by the arrival of data from a predecessor readying for a next processor [e.g., paragraph 73], wherein each MISD processor uses a timer for stamping the arrival time of incoming data [e.g., Fig. 5; paragraphs 79, 98 and 145].

Lee does not specifically teach using interrupt as triggering mechanism for synchronizing between the first core and second core.

However, in the same field of endeavor, Bass teaches synchronizing the passing of frames among the processors by monitoring input events, Data Buffers available for dispatch, Interrupts and Timers [e.g., col. 9, lines 31-32; col. 21, line 62- col. 22, line 5].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a plurality of timers for triggering Lee's data passing between MISD processors because: (1) interrupt is a well known technique for causing event triggering and synchronization among different processors, in particular when the processors are associated with different timers; and (2) using interrupt as triggering mechanism facilitates processors synchronization in Lee's data flow model in a sense that the execution of each processor may be triggered by its own local timer (i.e., without relying on a global clock).

17. As to claims 64-67, using Fig. 4 as an example, Lee demonstrates a data flow system where processors (such as 220a – 220c) are synchronized by the arrival of data from a predecessor readying for a next processor [e.g., paragraph 73], wherein each MISD processor uses a timer for stamping the arrival time of incoming data [e.g., Fig. 5; paragraphs 79, 98 and 145]. Bass teaches using interrupt as a triggering mechanism for causing the next processor to execute the available data. Such a triggering mechanism enables the processors to be clocked by their own local timers and uses a predecessor's timer to trigger interrupt for the next processor when data from the predecessor is available.

In light of the teachings of Lee and Bass, it is obvious that an ordinary skill in the art would be able to synchronize a plurality of processors as required in claims 64-67 because no matter how the different processors are mutually interconnected, the triggering mechanism between any processor pair is the same. That is: use a predecessor's timer to trigger interrupt for the next processor when data from the predecessor is available, which has been fully taught by Lee and Bass as described above.

18. Claims 50-55 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office Action and to include all of the limitations of the base claim and any intervening claims.

19. Applicant's arguments filed on 6/24/08 for claims 1-9 have been fully considered but they are not deemed to be persuasive.

20. Applicant argues in the remarks that: (1) Lee's MISD processors appear to be implemented using custom circuits or ASICs (as shown in Fig. 4) and Lee does not describe the MISD as being capable of performing DSP functions. (2) Lee does not teach that the different traffic management functions are performed within the same DSP integrated circuit. (3) Claim 5 requires no direct communication between the first core and the second core and claim 6 requires that communication between processors makes use of mailbox. However, according to Lee's Fig. 4, the MISD processors (e.g., 220a to 220b, and 220b to 220c) are directly connected, there is no

need for making use of mailbox in Lee's inter-processor communication. (4) There is no motivation for Lee to synchronize processors using an interrupt mechanism.

21. The examiner respectfully disagrees with Applicant's arguments.

As to point (1): Applicant is reminded that there is no clear definition as to what a DSP chip should look like or what are nominal "DSP functions" in Applicant's disclosure. For example, Applicant discussed several known DSP chips from single-core DSP such as TMS320C64xx series and Analog Devices' ADSP-TS20xS series to multi-core DSP such as Motorola's MSC8102, with the coupling of processing units ranging from tight (e.g., direct connections among single-core ALUs) to loose (e.g., indirect connection among multi-cores). It is unclear what characteristic of DSP architecture or DSP functions Applicant had in mind. Another example comes from the prior art Lee reference, where in paragraphs 8-12 Lee teaches that RISC processors are being used as graphic processors and DSPs. It is well known that RISC chip has been widely used in general-purpose computing. This latter example further blurs the borders of a DSP, if such borders clearly exist at all. Since the claim language of independent claims 1, 2 and 8-9 only requires that the DSP integrated circuit have "at least 128K bytes of on-chip memory", the term "DSP" or "digital signal processing" can only be viewed as Applicant's lexicography with an explicit memory capacity requirement. As such, the so called DSP processors have been properly mapped to Lee's MISD processors. It is further noted that Lee never mentions that the MISD processor is a custom circuits or ASICs. Fig. 4 is one example of Lee's multi-core network processor, which is properly mapped to Applicant's multi-core DSP in the claims.

As to point (2): In paragraph 29 Lee describes the network processor in Fig. 4 as having three MISD processors on which all the claimed traffic management functions are implemented [see paragraph 76]. Since the contemporary IC fabrication technology already can put multiple conventional board designs onto a single integrated circuit, one of an ordinary skill in the art would have no doubt at the fact that Lee's network processor (of Fig. 4) is or can be implemented on an integrated circuit unless Lee explicitly teaches away. Applicant is further noted that by requiring a multi-core DSP to be implemented on a single chip does not make the claimed subject matter more patentable because Applicant's invention is irrelevant to fabrication technology.

As to point (3): It is noted that MSC8102 is the only multi-core DSP Applicant described in the specification and Fig. 6 clearly shows that there are a plurality of buses interconnecting the four extended cores (SC140). As such, it is unclear why Applicant claims that no direct connection exists between the cores, and the core to core communications solely rely on mailboxes established external to these cores. If Applicant is meant to create his/her own version of multi-core DSP, then Applicant has not shown or proven that such new DSP architecture existed at the time of filing this instant application. On the other hand, although Lee's Fig.4 does show seemingly direct connections between the MISD processors, Lee also shows in Fig. 5 that there are communication units/buffers (such as 290 and 292) laid external to the MISD core [see 250, Fig. 5; paragraphs 83-84], wherein 292 has been properly mapped to the "mailbox" in claim 7 (see action item #16 of the previous office action). Thus, it depends on how one draws the borders of a MISD processor. If 290 and 292 of Fig. 5 are drawn outside the MISD processor, then an alternative Fig. 4 would show indirect connections between the processors.

As to point (4): Applicant is reminded that in the rejection of claim 7 the examiner cited a second reference, Bass, who teaches using interrupt mechanism for inter-processor synchronization. Since Lee teaches that the MISD is a data flow machine of which processors are triggered by availability of data [paragraph 73] and that each processor is associated with a local timer [e.g., paragraphs 98 and 145], it becomes obvious to one of ordinary skill in the art to use interrupt as a triggering mechanism between the processors for transferring data from one to the other because interrupt mechanism allows data transfer to occur between the involved processors when running on their own clocks.

For at least the foregoing reasons, it is submitted that the prior art of record reads on claims 1-9.

22. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

23. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Examiner note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the contest of the passage as taught by the prior art or disclosed by the Examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wen-Tai Lin whose telephone number is (571)272-3969. The examiner can normally be reached on Monday-Friday(8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(571) 273-8300 for official communications; and

(571) 273-3969 for status inquires draft communication.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wen-Tai Lin

August 31, 2008

/Wen-Tai Lin/

Primary Examiner, Art Unit 2154